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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,158	10/01/2003	Ming-Fang Wang	67,200-1160	8159

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TUNG & ASSOCIATES
Suite 120
838 W. Long Lake Road
Bloomfield Hills, MI 48302

EXAMINER

GEORGE, PATRICIA ANN

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/677,158

Applicant(s)

WANG ET AL.

Examiner

Patricia A. George

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9, 11, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. of US 6,803,275.

Park et al. disclosed all the limitations of claim 1 including a method for forming a gate oxide, of a high-k dielectric (col.6, l.23-58) stack (fig.2, 32/30 and), and treating it to reduce the oxygen vacancies (col.7, l.39-40), which is written on "plasma treatment". Park disclosed an improvement to the oxide layer by minimizing charge leakage paths through the bottom into the channel region (col.4, 63-65), written on "to improve electric performance characteristics." Park's gate dielectric layer is on a silicon substrate (fig. 1, 15 and col.5, l.61); and under a polysilicon layer (fig.1, 22 and col.19, l.66, note typo – control gate electrode formerly cited in l.61 as part #22 is cited as part 24 in l. 64, further examination of figure 1, makes it clear that the control gate electrode, is in fact part 22.). Park disclosed lithographic patterning and etching process to define the stacked gate structure (col.19, l.58-60). Park illustrates at least one plasma treatment in figure 7,

Art Unit: 1765

step S703. Park disclosed the decoupled plasma oxidation (col.10, l.16-17) uses a gas mixture of oxygen, and may include argon (col.12, l.24-25).

As for claims 2-4, Park disclosed step (b) an annealing process (col.10, l.17), to follow step (a) the plasma treatment. Park disclosed annealing with oxygen and an inert gas, such as nitrogen at a temperature of 600 degree C to 1100 degree C (col.12, l.41-44). In regard to the temperatures, times, and gasses used, Park discloses, they are known to those skilled in the art, dependent and interdependent on several other process parameters (col.9, l.1-7).

As for claim 5, Park disclosed the gate dielectric layer stack comprises a bottom layer (28) of SiO₂ (col.6, l.11), which is over the silicon substrate (see fig. 1).

As to claim 6, Park disclosed suitable gate dielectric high-K materials in column 6, lines 36-58, which include all types listed in the claimed group.

As to claim 7, Park disclosed, wherein the dielectric layer stack consists of a bottom SiO₂ layer (see discussion of claim 6) and a high-k dielectric material formed by reacting hafnium tetra-t-buoxide with O₂ or N₂O (col.17, 58-59), which is written on "an overlying hafnium oxide layer."

As for claim 9, see the discussion above, to claim 1.

As for claims 11 and 12, Park discloses a variety of ranges for the plasma treatment, including 5 – 100 mTorr (col.12, l.31-31), which abuts the claimed range 100mTorr to 10 Torr; and 5-100 Torr which encompasses and overlaps the claimed ranges.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Sarigiannis et al. of 2004/0152304.

As to claim 8, Park disclosed the high-k dielectric materials may be formed by any suitable CVD method, known in the art including ALD (ALCVD) (col.17, l.63-65).

Park does not disclose the process temperature for an ALD deposition.

Sarigiannis et al. teaches an ALD deposition temperature of 200 degree C, (para.4, l.11), which is within the claimed range of less than about 300 degree C".

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include a process temperature for ALD deposition, as Sarigiannis, when forming the gate structure, of Park, because Sarigiannis teaches it can be advantageous.

Claim Rejections - 35 USC § 103

Claims 10, 13 - 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (see discussion above), in view of Baum et al. of US 2002/0175393.

Park does not disclosed the claimed time of the plasma treatment which is “carried out for a period of between about 10 minutes and about 90 minutes”, as in claim 10. Park discloses all of the limitations of claim 13, with the exception of the plasma treatment improves flatband Voltage and threshold Voltage characteristics of a CMOS device.

See table 2, where Baum et al. teaches a time of 10-30 minutes for plasma treatment of hafnium, which is encompassed by the range of claim 10.

In the background of the invention, Baum teaches plasma treatment minimizes carbon incorporation into dielectric thin films, degrades leakage, dielectric constant, and overall electrical performance of the thin film, which is written on “improves flatband Voltage and threshold Voltage characteristics of a CMOS device (para.13 and 21).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to use the process parameters for plasma treatment, as Baum, when forming the dielectric gate stack, of Park, because Baum teaches it minimizes carbon incorporation into the dielectric thin film, which degrades leakage, dielectric constant, and overall electrical performance of the thin film.

As to claims 14 and 15, see discussion above on claims 2-4.

As to claim 16, see discussion above to claim 7.

As to claim 17, see discussion above to claim 6.

As to claim 18, see discussion above to claim 7.

As to claim 20, see discussion above to claims 11 and 12.

Claim Rejections - 35 USC § 103

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. and Baum et al. (see discussion above) in further view of Possin et al. of US 5,282,546.

As to claim 19, Park fails to disclose a step where in the gate structure is treated with a hydrogen (H.sub.2) source gas.

Possin teaches, hydrogen treatment of a dielectric gate stack with polysilicon on top (see abstract), as in claim 19, for improved electrical performance (col.2, l.26).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of forming a gate stack, of Park, to include to an additional step of treating plasma source gas of Hydrogen, because Possin teaches it stabilizes the surface of the interface by yielding fewer defects, resulting in improved electrical performance, a results that increases profit. One of ordinary skill desiring increased electrical performance would be motivated to include an additional plasma treatment with hydrogen source gas.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US 6,740,605 and US 2002/0175393.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patty George whose telephone number is (571) 272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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Patricia A George
Examiner
Art Unit 1765

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER

